

In the Drawings:

Please replace drawing sheets 3-4 (showing Figs. 2d-2i) with the newly submitted figures attached herewith on separate sheets.

REMARKS

The Examiner is thanked for the thorough examination of the present application, the allowance of claims 29-32, and the indication that claims 25 and 26 contain allowable subject matter. This response is in response to the Office Action of Sep. 9, 2005.

Priority

The Office Action indicates that this application should make proper reference, in the specification, to the parent application. Applicants agree. In fact, this reference was made in the Preliminary Amendment filed (by the former attorney) on April 12, 2004. In that Preliminary Amendment, the present specification was amended (immediately following the title of the invention on page 1) to add the following text:

This is a division of Patent Application serial number 10/295,157, filing date 11/15/02, Novel Multi-Level (4 State/2-Bit) Stacked Gate Flash Memory Cell, assigned to the same assignee as the present invention, which is herein incorporated by reference in its entirety.

No further priority reference is believed to be required.

Amendment to the Specification and Drawings

Applicants have amended the specification to change reference numeral 120 to 122, at the bottom of page 14. Applicants also insert, in Figs. 2e-2h, a symbol of 122 to indicate a tunnel oxide and accordingly amends the specification in pertinent part. These amendments add no new matter to the present application.

Response To Claim Rejections Under 35 U.S.C. §112, Second Paragraph

Claim 21 was rejected as allegedly unclear as to whether thickness or temperature is claimed therein. Applicant amends claim 21 by changing "600 to 1100°C" into "150 to 250 Å." Support of this thickness limitation can be found at least in page 15 of the original specification and, therefore, adds no new matter to the application. Applicants submit that the rejection under 35 U.S.C. §112, 2nd paragraph for claim 21 has been overcome by this amendment.

Response To Claim Rejections Under 35 U.S.C. §102

Claims 19-20, 22-24, and 27-28 stand rejected under 35 U.S.C. §102(c) as allegedly anticipated by *Vora* (U.S. Patent No. 6,897,520). Applicants respectfully traverse this rejection on the ground that *Vora* does not disclose, teach, or suggest all of the claimed elements.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See e.g., In re Paulsen*, 30 F.3d 1475, 31 USPQ 2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ 2d 1655 (Fed. Cir. 1990).

Independent claim 19 recites:

19. A multi-level, multi-bit stacked gate flash memory cell structure comprising:

floating gate spacers having convex walls facing each other, and vertical outside walls;

a conformal dielectric layer covering said convex walls of said floating gate spacers;

a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer; and

insulative spacers formed on said vertical outside walls of said floating gates.

(*Emphasis added*). *Vora* does not disclose, teach, or suggest at least the feature emphasized above. Therefore, the rejection under 35 U.S.C. §102(e) cannot properly be sustained and should be withdrawn.

In Page 5, the Office Action referred to material 20 & 20' in Fig. 5 of *Vora* as the insulative spacers of claim 19. This reflects a misapplication of *Vora*. In this regard, the material 20 and 20' are not insulative spacers, however. Instead, and referring to material 20 and 20' in Fig. 5 and their equivalent material 100 in intermediate Fig. 20B, *Vora* uses terms such as a thin annular oxide layer (Col. 2, Ln. 37), a gate oxide (Col. 4, Ln. 34), and a thin gate oxide layer (Col. 7, Ln. 41 and Col. 11, Ln 58). As well known in the art, a gate oxide layer cannot be a "spacer." If *Vora* thought of a gate oxide layer as a spacer, *Vora* should consistently apply the term "spacer" to the gate oxide. In fact, *Vora* does understand the difference, so the term "spacer" is never used in *Vora* for a gate oxide layer. Instead, the term "spacer" in *Vora* is specially spared and consistently used for the material 32 and 32' of Fig. 5 (Col. 4, Ln. 19) and the material 114 of Fig. 26B (Col. 9, Ln. 7-23, and 20-22, and Col. 12, Ln. 42-44). Therefore, material 20 and 20' in *Vora* are not spacers.

Instead, the spacers disclosed by *Vora* are symbolized as 32, 32' in Fig. 5 or 114 in Figs. 26-33, and none of them are formed on the vertical outside walls of the floating gates as required in the original claim 19. Since at least one feature in claim 19 is not disclosed by *Vora*, the rejection under 35 U.S.C. §102(e) should be withdrawn and claim 19 should be allowable over the prior art of record.

As independent claim 19 is allowable over the prior art of record, then its dependent claims 20-23 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 19. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

With regard to independent claim 24, claim 24 recites:

24. A multi-level, multi-bit stacked gate flash memory cell structure, comprising:
two floating gates on an insulating layer on a substrate, having opposite sidewalls facing each other;
a conformal dielectric layer covering opposite sidewalls of the two floating gates;
a control gate therebetween the opposite sidewalls of the two floating gates with intervening the conformal dielectric layer; and
two insulative spacers covering outside walls of the two floating gates."

(Emphasis added)

Based upon the same argument that was set for in connection with claim 19, *Vora* does not disclose, teach, or suggest the emphasized feature in claim 24. Therefore, the rejection under 35 U.S.C. §102(e) should be withdrawn and claim 24 should be allowable over the prior art of record.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 19-32 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic

conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

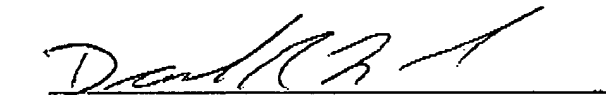
CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By:


Daniel R. McClure
Registration No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500

3/7 Annotated Drawing Sheet

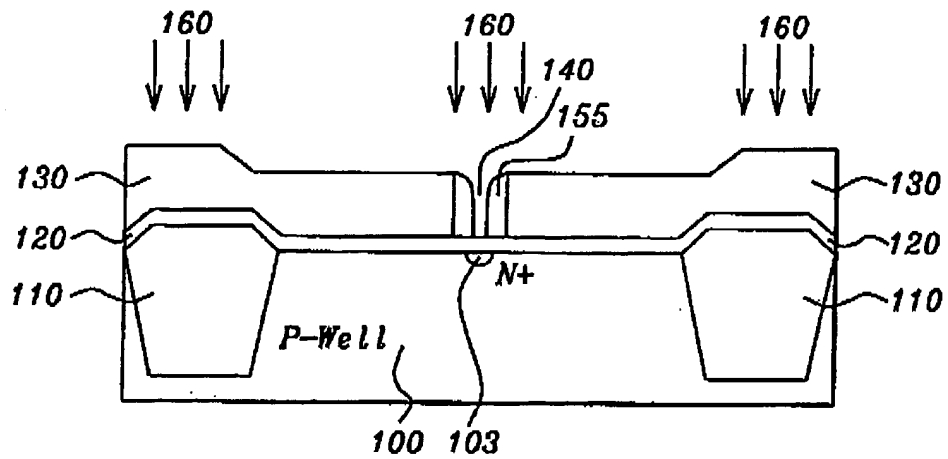


FIG. 2d

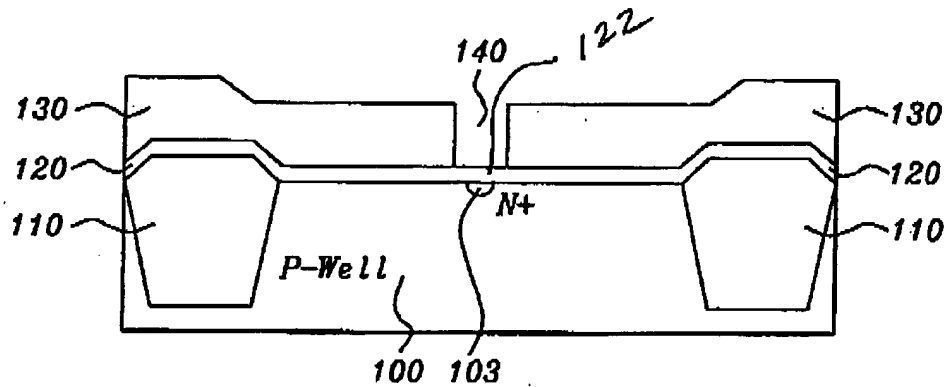


FIG. 2e

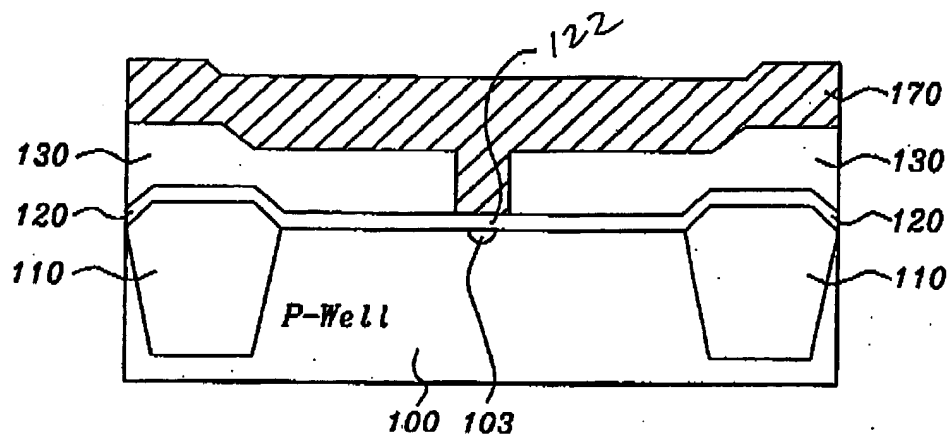


FIG. 2f

4/7 Annotated Drawing Sheet

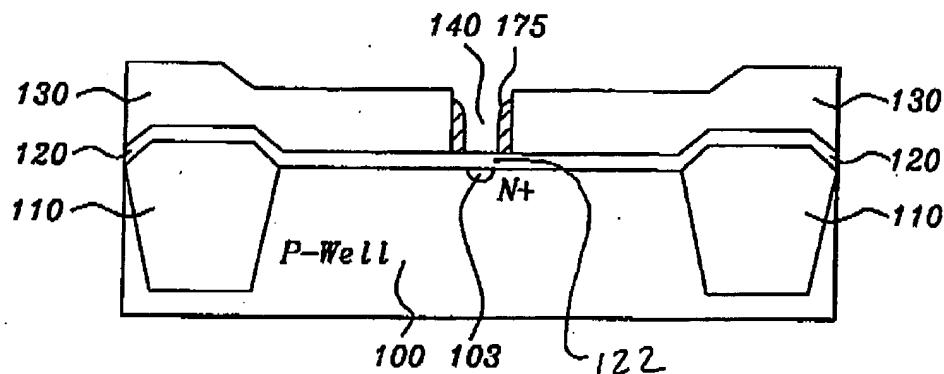


FIG. 2g

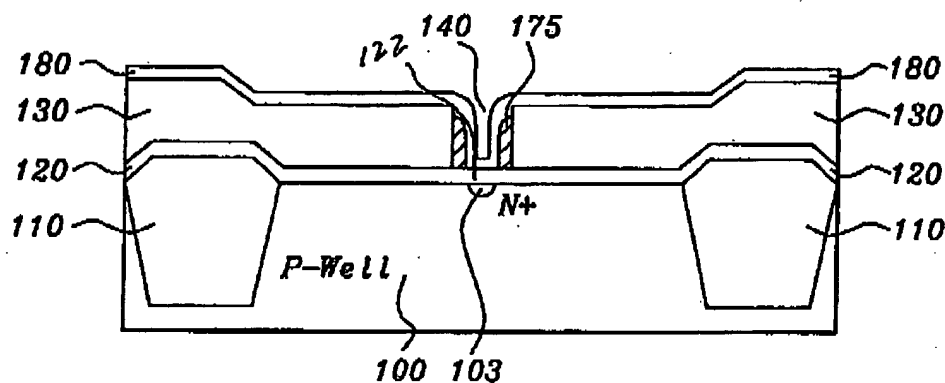


FIG. 2h

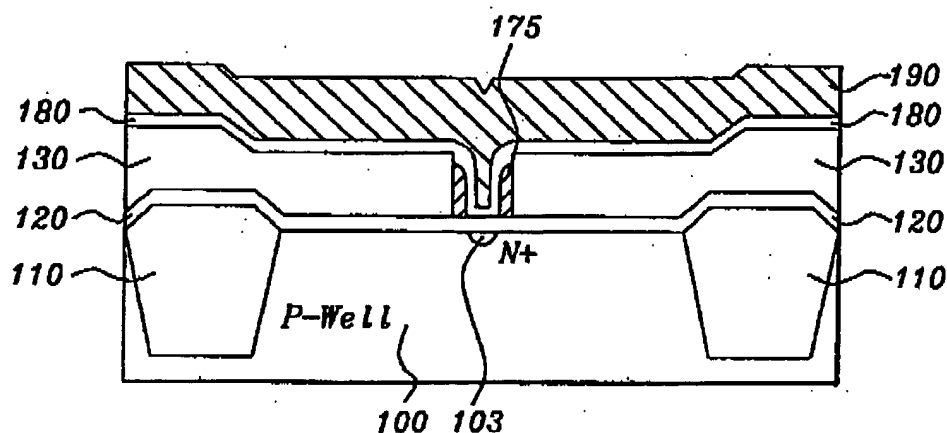


FIG. 2i